UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,085	11/01/2001	William John Goetzinger	ROC920010202US1	2023

31647 7590 10/05/2005

DUGAN & DUGAN, P.C.
55 SOUTH BROADWAY
TARRYTOWN, NY 10591

EXAMINER	
SONI, DEEPAK H	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,085	GOETZINGER ET AL.	
	Examiner	Art Unit	
	Deepak Soni	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *01 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449.or PTO/SB/08) Paper No(s)/Mail Date *sep.13,05,sep12,05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

Requesting update of co-pending application on page 1 of the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless -

   (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **5,13,8 and16** are rejected under 35 U.S.C. 102(e) as being anticipated by Meier et al. (U.S. 6,481,251). The Meier et al. reference teaches all of the limitations of the listed claim with reasoning that follows. Regarding claims **5 and13** "examining an empty indicator associated with the scheduling queue;" Meier et al. anticipates empty indication for store queue as spoken of column 13, lines 66-67 and column 14, lines 1-4 "refraining from searching the scheduling queue if the empty indicator indicates that the scheduling queue is empty; searching the scheduling queue if the empty indicator indicates that the scheduling queue is not

empty; detaching from the scheduling queue a winning flow found in the searching step." Meier et al. anticipates store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10.

Regard claims **8 and16**, "checking a bit in a register" Meier et al. anticipates the empty indication may be a bit indicating empty when set and indicating not empty when clear. Column 14, lines 5 and 6.

Regarding claim **24**, Meier et al. discloses all the limitations of claim 24 as discussed with claim 13. It should be noted that claim 24 is simply the computer program containing the methods of claim 13, and it should be obvious to have a medium readable by a computer to implement the same steps for the method of claim 13.

3. Claim **9** is rejected under 35 U.S.C. 102 (e) as being anticipated by Naven et al. (U.S. 6,810,043), hereinafter referred to as Naven. The Naven et al.

reference teaches all of the limitations of the listed claim with reasoning that follows.

Regarding claim **9**, "attaching a flow to the scheduling queue;" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61. "Placing an empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-4,19 and 21,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 1,2 and 3 in view of Meier et al. (U.S. 6,481,251).

Regarding claim **1**, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more schedules queues, each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. teaches empty indication in the empty register indicates that the store queue is empty column 14, lines 2-4. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of Prior Art in order to indicate weather the respective scheduling queue is empty as spoken of on column 14, lines 2-4 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, then the cycle may be wasted.

Regarding claim **2**, Meier et al. further discloses empty indication may be a bit indicating empty when set and indicating not empty when clear, as stated in column 14, lines 5-6.

Regarding claim **3**, Applicant's admitted Prior Art further discloses one or more schedule queues 42 includes plurality of scheduling queues as shown in Figure 2. Prior Art fails to disclose empty indicators include a plurality of empty indicators. However, Meier et al. Figure 5, illustrates store queue assignment circuit 60 in response to completion of one or more stores. Additionally, store queue number assignment circuit 60 determines if the head store queues number equals the tail store queue number. If so, the empty indication in empty register 65 is set to indicate empty as stated in column 14, lines 24-48. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to use plurality of empty indicators of Meier et al. along with plurality of scheduling queues of Admitted Prior Art Figure 2. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, then the cycle may be wasted.

Regarding claim **4**, Applicant's admitted Prior Art further discloses each scheduling queue 42 includes 512 slots 48 to which flows are attachable as shown in Figure 2 and 3.

Regarding claim **19,** "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a

respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3 Prior Art fails to teach "examining an empty indicator associated with the first scheduling queue;" Meier et al. teaches empty indication for store queue as spoken of column 13, lines 66-67 and column 14, lines 1-4 "refraining from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; and detach from the first scheduling queue a winning flow found in the search of the first scheduling queue." However Meier et al. teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement

empty indicator of Meier et al. in schedule queue of Prior Art in order to indicate weather the respective scheduling queue is empty as spoken of on column 14, line 2-4 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

Regarding claim **21**, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues; each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty "However, Meier et al. teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3. Prior Art fails to teach "examine an empty indicator associated with a first scheduling queue; refrain from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; search the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; if a winning flow is found by the search of the first scheduling queue, detach the winning flow from the first scheduling queue; if no flow is found by the search of the first scheduling queue, place the empty indicator in a condition to indicate that the first scheduling queue is empty." Meier et al. teaches store queue control

circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of Prior Art in to search or not to search if empty indicator indicate empty or not empty as spoken of on column 14, line 2-6 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

5. Claims **10-12, 17,18, and 23**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Naven et al. (U.S. 6,810,043), hereinafter referred to as Naven.

   Regarding claim **10**, Naven discloses scheduling circuitry comprising a master calendar and a slave calendar in which to schedule cell

transmissions (a scheduler for a network processor, the scheduler comprising a scheduling queue in which flows are en-queued, Abstract). Naven however fails to disclose the specific limitations of claim 10, more specifically the formula of CP + ((WF x FS) / SF). Naven however discloses using known techniques are used in which the "the next scheduled time" or NST at which the next cell for the specified VC is to be transmitted is calculated (column 5 lines 5-8) and further discloses that if the NST is within the scheduling range SR of the master calendar (schedule queues), a new entry for the specified VC is made in an appropriate one of the storage locations of the master calendar, and if on the other hand, the NST is outside the scheduling range SR of the master calendar, the specified VC is instead entered in one of the storage locations of the slave calendar (sub-queues), which storage location is also used to store the NST for the specified VC (the flow appointed for en-queuing is en-queued to the scheduling queue if the value of the expression is less than a range of the scheduling queue and the flow appointed for en-queuing is en-queued to the sub-queue if the value of the expression is greater than a arrange of the scheduling queue, column lines 19-29). Naven thus provides the motivation for a need for a formula to effectively calculate the NST. It should be obvious to incorporate the well known weighted fair queue technique (CP + (WF x FS) / SF) disclosed by the applicant into the scheduling circuitry to schedule cell

transmission including a master calendar and a slave calendar disclosed by Naven in order to effectively calculate the NST.

Regarding claim **11**, "setting a bit in a register" Naven discloses when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein. Column 8, lines 24-26.

Regarding claim **12**, "resetting a bit in a register" Naven discloses if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry column 8, lines 26-28.

Regarding claim **17**, "if the detaching step is performed, a further search of the scheduling queue is performed to determine whether any flows are en-queued in the scheduling queue other than the flow detached in the detaching step." Naven discloses when a bit in the word 22 is set to 1 this denotes that the corresponding storage location 2 has at least one VC entered therein. If the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty" i.e. does not contain a valid entry. Column 8, lines 24-28.

Regarding claim **18**, "the empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step." Naven discloses if the bit is 0, on the other hand, this denotes that the

corresponding storage location 2 is "empty", i.e. does not contain a valid entry column 8, lines 26-28.

Regarding claim **23**, Naven et al. discloses all the limitations of claim 23 as discussed with claim 9. It should be noted that claim 23 is simply the computer program containing the methods of claim 9, and it should be obvious to have a medium readable by a computer to implement the same steps for the method of claim 9.

6. Claims **6 and14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (U.S. 6,481,251) and in view of Lyons et al. (Third New Zealand ATM and Broadband Workshop: Title- Estimating Clock Speeds for the ATMSWITCH Architecture).

Regarding claims **6 and14**, Meier et al. teaches empty indicator associated with scheduling queue, refraining from searching the scheduling queue if the empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claim 5 and 13). Meier does not teach, "selecting the scheduling queue from among a plurality of scheduling queues in a round robin process." Lyons et al. teaches round robin process in ATMSWITCH, At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. and searching the scheduling queue in a round robin server as in Lyons et al. in moves around the circular queue removing a cell from the current cell queue whenever the output port becomes free, and moving on to next

queue in time for the next output slot. Column 3, Paragraph 4 lines 6-11 under The ATMSWITCH.

7. Claims **7 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (U.S. 6,481,251) and in view of Lyons et al. (Third New Zealand ATM and Broadband Workshop: Title- Estimating Clock Speeds for the ATMSWITCH Architecture) and in further view of Naven et al.

   Regarding claim **7 and15**, Meier teaches empty indicator associated with scheduling queue, refraining from searching the scheduling queue if the empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claim 5 and 13) and Lyons teaches round robin process (see claim 6 and 14). Meier et al. and Lyons et al does not teach "searching step includes a plurality of sub-queues includes in the scheduling queue, the sub-queues having mutually different respective ranges and resolutions." However in further view of Naven et al., Naven teaches that the master calendar (scheduling queue) and slave calendar (sub-queues) are plurality of storage locations corresponding respectively to a succession of time slots (column 4 lines 44-45). It can also be seen from figure 2 that the slave calendar and master calendar have a different number of time slots. It should be obvious to a person skilled in the art given these references to have different ranges and resolutions for sub-queues. A motivation for doing so would be the master calendar and slave calendar have the different

range and resolution of slots (the scheduling queue has different number of slots that is different than a number slots of the sub-queue, 7 and 2 of figure 2).

8. Claim **20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1,2 and 3 in view of Meier et al. (U.S. 6,481,251) and in further view of Naven et al. (U.S. 6,810,043).

Regarding claim **20**, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced" Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42. Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." However, Meier et al. teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3 Prior Art and Meier et al. fails to teach "attach a flow to the first scheduling queue;" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61. "Place an empty indicator associated with the first scheduling queue in a condition to indicate that the first scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit

word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier et al. in schedule queue of Prior Art in order to indicate weather the respective scheduling queue is not empty as spoken of on column 14, line 2-6 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

9. Claims **22 and 24,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (U.S. 6,481,251).

   Regarding claim **22**, Meier et al. discloses all the limitations of claim 22 as discussed with claim 5. It should be noted that claim 22 is simply the computer program containing the methods of claim 5, and it should be obvious to have a medium readable by a computer to implement the same steps for the method of claim 5.

   Regarding claim **24**, Meier et al. discloses all the limitations of claim 24 as discussed with claim 13. It should be noted that claim 24 is simply the computer program containing the methods of claim 13, and it should be obvious to have a medium readable by a computer to implement the same steps for the method of claim 13.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deepak Soni whose telephone number is 571-272-2816. The examiner can normally be reached on 9:00Am - 5:00Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Deepak Soni
Examiner
Art Unit 2666

DS

Seema S. Rao 10/3/05
SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600